Amendments to the Claims:

The following listing of claims will replace all prior versions, and listings, of claims in the application:

1-25. (Canceled)

26. (New) A ferroelectric memory, comprising:

a substrate;

a passive matrix array in which memory cells formed of ferroelectric capacitors are arranged; and

a peripheral circuit for the passive matrix array,

wherein the passive matrix array is formed on a first microstructure, the peripheral circuit being formed on a second microstructure, and first and second recess portions are formed in the substrate, and the first microstructure is provided in the first recess portion and the second microstructure is provided in the second recess portion.

27. (New) The ferroelectric memory according to claim 26, wherein the first recess portion and the second recess portion are formed adjacent to each other, and the first microstructure and the second microstructure are arranged so that they come in contact with each other.

28. (New) The ferroelectric memory according to claim 27, wherein the second microstructure includes a word line microstructure that has a word line driver circuit and a bit line microstructure that has a bit line driver circuit, and the word line microstructure and the bit line microstructure are respectively provided in two second recess portions which are formed adjacent to the first recess portion.

29. (New) The ferroelectric memory according to claim 26, wherein a plurality of the first microstructures are provided in layers in the first recess portion.

30. (New) The ferroelectric memory according to claim 29, wherein a drain wiring is provided along a sidewall of the first recess portion.

31. (New) The ferroelectric memory according to claim 30, wherein a planarized film is formed between the first microstructures.

32. (New) A ferroelectric memory, comprising:

a substrate;

a passive matrix array in which memory cells formed of ferroelectric capacitors are arranged; and

a peripheral circuit for the passive matrix array,

wherein the passive matrix array is formed on a first microstructure, and the peripheral circuit is formed on a second microstructure, and a second recess portion is formed in the substrate, the second microstructure is larger than the first microstructure and provided in the second recess portion, a first recess portion is formed in the second microstructure and the first microstructure is provided in the first recess portion of the second microstructure.